Assignment 6b: Memory-Mapped Address Decoding, Part II

out Wed Oct 15
due Mon Oct 20

Note

This problem supplements Assignment 6. Both this problem and the previously distributed Assignment 6 are now due Monday, October 20.

8K RAM for 68HC11

Assume you have an 8K static RAM, the CY6264, as shown in the following data sheet.

This RAM is to be mapped into the 68HC11's address space in the range 0x8000 to 0xBFFF.

Design a circuit to accomplish this, and draw a schematic to represent it.

Your schematic should include the 68HC11, a 74HC373 transparent latch, the CY6264 static RAM chip, and any other gates or components you deem necessary.

Please note:

1. You do not need to build the circuit, just draw the schematic.
2. Include a brief (one-paragraph) written description of your design.
3. Make sure to use only parts that are available in your kit.