ASSIGNMENT 8: PIPELINING, CACHES, BRANCH PREDICTION

due Wed, Nov 27

Problem 1.

On page 258 of the text, Tanenbaum shows how the microcode for the *swap* instruction is rewritten into a series of *microsteps*, enabling it to run on the pipelined Mic-3 machine.

Based the discussion in the text and this example, create a microstepped table for the *iadd* instruction. Use the Mic-2 control store definition as a source (pages 254–255).

Problem 2.

Per above, create the microstep table for the *istore* instruction.

Problem 3.

Based on your two designs, illustrate how the following IJVM code works its way through the Mic-3:

```
iadd
istore 0
```

How many cycles does this take? Based on the discussion of the speed of the pipelined Mic-3 vs. the Mic-2, how much faster will this two-instruction sequence be?

Problem 4.

Answer question 26 on page 301.

Problem 5.

Answer question 30 on page 302.