91.305 COMPUTER ARCHITECTURE
REVIEW NOTES, FALL 2002

Assignment 1 – what is a computer, orders of magnitude of computation, bits, bytes.

Assignment 2 – logic levels (0v = 0, 5v = 1), circuit construction/testing skills, inputs and outputs, reading data sheets, combinational logic functions AND/OR/NOT/XOR, De Morgan's law (AND followed by OR == NAND followed by NAND), positive-true vs. negative-true signals, counters, edge-triggered (clocked) vs. level-sensitive (reset) inputs, ganging counters, flip-flops, inverters and feedback loops, finite state machines: state transition diagrams, state assignments, state tables, state equations, minimization, complete state machine implementation (latch + combo logic/ROM, where combo logic takes current state+sensors as inputs, and computes next state+control signals as outputs).

Assignment 3 – wiring and booting the 68HC11 microcontroller, assembly vs. machine language, HC11 instruction set, programming the HC11, cycle counting, period vs. frequency, generating tones with machine code, ASCII character set, printing characters to the serial line & displaying them on a console terminal.

Assignment 4 – analog-to-decimal conversion, using a photocell light sensor, more HC11 programming (making a loop; using registers as loop counters).

[mid term covered content to this point.]

Assignment 5 – memory-mapped I/O, address decoding, HC138 3-to-8 decoder.

Assignment 6 – ALU and its control signals, Mic-1 design including: phases of operation and timing (Δw, Δx, Δy, Δz); B bus registers and associated selector; C bus registers and associated bit field; microinstruction register (MIR); memory interface (MAR, MDR, PC, and MBR(U) registers); jump circuitry/logic (JAMN/Z bits, addr bits from MIR, MPC register), IJVM instruction set (stack oriented design; special registers (CPP, TOS, LV)). Also (in class): INVOKEVIRTUAL method call; register machine (HC11, Pentium) vs stack machine (IJVM).

Assignment 7 – using the Mic-1 simulator tools, writing microcode for the Mic-1 design.

Assignment 8 – pipelined versions of the Mic-1, writing microcode for pipelined Mic-4, caches, branch prediction. Also (in class): prefetching with an instruction fetch unit, adding a 2nd bus to the ALU, direct-mapped vs. set-associative cache designs, static vs. dynamic branch prediction & methods, out-of-order execution & register renaming, speculative execution; comparison of picoJava, Pentium II, and SPARC designs, RISC vs. CISC, interpreting marketing claims.

Assignment 9 – Pentium ISA, C compilation to assembly including if-else, while, and for loop forms, use of stack for procedure calls, arguments, local variables, and the frame ptr, use of `objdump` and `gdb` to examine and interact with binary executables.

Important Readings – PC Processor Microarchitecture report, Chapter 3 excerpt from Bryant/O'Hallaron.